REMARKS

Favorable reconsideration of this application in light of the above mentioned amendments and the following remarks is respectfully requested.

Claims 1-9, 14, 23, 25, 27-28, 49-57, 63-66, 77-79 are amended herein.

New claim 80 has been added herein as listed above.

The objections that Examiner provided with respect to the drawings have been duly observed by the Applicant and have been corrected in the attached figures. Approval by the examiner is kindly requested.

The objections that Examiner provided with respect to the informalities in the text have been duly observed by the Applicant and have been corrected.

Examiner J. Garcia is thanked for her thorough examination of the Prior Art.

The invention teaches a method for forming a top for high performance integrated circuits by forming an integrated circuit containing a plurality of devices formed with an overlaying interconnecting metallization structure connected to the devices that contains a plurality of first metal lines in one or more layers. A layer of passivation is deposited over the interconnecting metallization structure over which an insulating, separating layer is deposited. Openings are formed through the insulating, separating layer and the passivation layer to expose upper metal portions of the overlaying interconnecting metallization structure. Metal contacts are deposited in the openings and a top metallization system is formed that is connected to the overlaying interconnecting metallization structure. The top metallization system contains a plurality of top metal lines, in one or more layers, whereby each of the top metal lines have a width substantially greater than the first metal lines.

Claim Rejections - 37 CFR 1.75(c)

Claims 3-9 and 50-55 have been objected to by Examiner under 37 CFR 1.75(c) as being improper dependent form for failing to further limit the subject matter of a previous claim. The subject matter that is further specified in claims 3-8 and

claims 50-55 is the specific functionality, such as power planes, signal lines and the like, of the top metallization system. The subject matter that is further specified in claim 9 is the functional characteristic of the overlaying interconnecting metallization structure whereby this metallization structure can be extended to include contact points. We therefore respectfully submit that dependent claims 3-9 and claims 50-55 do in fact further limit the processes of the independent claim 1 and claim 49 and therefore respectfully request reconsideration of claims 3-9 and claims 50-55.

Claim Rejections - 35 U.S.C. 103(a)

Examiner has rejected claims 1-28 and 49-79 under 35 U.S.C. 103(a) as being unpatentable over Bandyopadhyay et al. in combination with Yamada '778, Yamada '020, Wolf and Cronin.

Reconsideration of the rejection of claims 1-28 and 49-79 under 35 U.S.C. 103(a) is respectfully requested based on the following arguments.

While Bandyopadhyay et al. '776 do disclose forming an integrated circuit containing a plurality of devices that is formed in and on a semiconductor substrate, Bandyopadhyay et al.

differs in very significant aspects from the present claimed invention. Bandyopadhyay et al. provides for a multilevel interconnect structure that includes at least three levels of interconnect metal whereby the essential purpose of the Bandyopadhyay et al. disclosure is to achieve high packaging density concurrent with reduced parasitic capacitances. The Bandyopadhyay et al. method applies, for this purpose, and arranged within the three levels of metal interconnect lines, a staggered format of interconnect line layout provided in separate horizontal and vertical planes. The main emphasis of the method that is provided by Bandyopadhyay et al. is on staggering the metal conductors, this staggering of metal lines is accomplished in three levels of interconnect whereby the three levels are required in order to provide adequate flexibility in arranging the lines. The process and structure of the present invention by contrast addresses the formation of two metallization systems that are formed on top of and overlaying conventional semiconductor devices. Each of the two metallization systems of the present invention form a metal interconnect system whereby the lower layer (the metallization systems closest to the conventional semiconductor device) typically contains (for reasons of device performance) fine line interconnect lines that are embedded in a thin layer of inorganic dielectric and that are connected to the conventional

semiconductor device by applying conventional IC interconnect methodologies. The upper metallization system of the invention contains wider, more robust interconnect lines that are embedded in a thick layer of polymer. The two metallization systems of the invention are separated by a continuous layer of passivation or polymer, the passivation layer of the invention may contain silicon nitride. The continuous passivation layer serves to protect the under lying devices from moisture and foreign particles and mobile ions, this allows for the creation of coarse and robust metal that forms the overlying metal interconnects by the application of more cost effective methods of device fabrication such as less stringent clean room environment and simplified or less stringent processing environments and conditions. It is clear from the processes and method of the present invention that these processes lead to the objectives of the present invention, objectives that are fundamentally different and considerably wider in scope than the previously highlighted objectives that are pursued by Bandyopadhyay et al. From the above indicated methods and structure of the present invention it is clear that the present invention is aimed at and satisfies its stated objectives such as the reduction of resistive voltage drop of the power supply lines that connect the IC to surrounding circuitry or circuit components, the reduction of the RC delay constant of the signal

paths of high performance IC's, facilitating the application of IC's of reduced size and increased circuit density, facilitating and enhancing the application of low resistor conductor metals, the facilitation of connecting of high-performance IC's to power buses, and the like, objectives that have all been stated and further highlighted in the application of the present invention. A few of the objective of the present invention have been repeated at this time in order to further demonstrate the broad scope of the present invention and the significant difference in the processes and design of the present invention when compared with the method that has been provided by Bandyopadhyay et al.

Also, the present invention suggests the use of silicon nitride to serve as the passivation layer that separates the previously indicated upper metallization system of the method of the invention from the lower metallization system of the method of the invention. Bandyopadhyay et al. does make use of silicon nitride in the method of his invention but only to the limited extend of using silicon nitride as an etch stop layer whereby only a small portion of silicon nitride remains in place under the second metallization system of metal. The passivation layer of the present invention separates over the entire length the upper metallization system of the invention from the lower metallization system of the invention.

The essential points of difference between the present invention and the method that is provided by Bandyopadhyay et al. can be highlighted as follows:

- Bandyopadhyay et al. does not disclose the function of a continuous passivation layer as highlighted above for the present invention and specifically does not provide for the application of silicon nitride in the function of a passivation layer
- Bandyopadhyay et al. does not disclose the use of a composite material of PECVD oxide (0.15 - 2.0 um thick) over which a layer of PECVD nitride (0.5 - 2.0 um thick) is deposited for the composition of the passivation layer
- the present invention does not create plug conductors nor uses nitride as an etch stop as provided by Bandyopadhyay et al.
- Bandyopadhyay et al. do not provide for a thick layer of polymer or of benzocyclobutene that is used as an insulating layer in the upper level of the metal interconnect systems of the present invention, this thick layer of polymer is used for planarization and for the reduction of parasitic capacitances
- Bandyopadhyay et al. do not claim a two level metal interconnect system

- Bandyopadhyay et al. do not embed more robust metal interconnects of the upper level thick layer of polymer of the invention
- Bandyopadhyay et al. does not provide for a two level interconnect system that uses wide and more robust metal in the upper level and fine, thin metal in the lower level of metal interconnects
- Bandyopadhyay et al. do not provide for a two level interconnect system that is separated by a transition layer of passivation material
- Bandyopadhyay et al. do not provide for a completed fine-line system below the layer of passivation while the present invention provides for a completed fine-line scheme of conducting lines below the layer of passivation, and
- Bandyopadhyay et al. is aimed at fine-line interconnects, the present invention provides for robust interconnects.

Yamada '778 provides a method of creating a compound layer of dielectric that separates a pattern of interconnect lines whereby the first layer contains a silicon oxide (SiO_2) film and the second layer contains silicon fluoride oxide (SiFO). Yamada '778 essentially provides an etching procedure that is applied to the compound layer of dielectric using the lower layer as an etch stop for the upper layer (the upper layer is etched using a

low fluorine gas content) with the overall objective of creating a pattern of interconnect lines that has low parasitic coupling thereby improving high speed device performance. The Yamada '778 objective and methods are therefore fundamentally different from the present claimed invention, because the Yamada '778 method provides for a semiconductor device structure that implements a silicon fluoride oxide film as an interlayer insulating film to reduce the dielectric constant of the interlayer insulating film and has objectives that are considerably different from the objectives of the present invention, resulting in a device structure that is considerably simpler and more limited in wiring capabilities than the device of the present invention. The device of the present invention is aimed at advancing the state of the art as it applies to increased device packaging densities without incurring penalties of electrical performance for the devices and therefore results in a device package that is considerably more complex and expandable when compared with the Yamada '778 method. The Yamada '020 method provides for fine-line interconnects which is at variance with the present invention that provides for robust interconnects.

Yamaha '020 has as objective the reduction or elimination of defects in aluminum wires that are used for interconnect lines. Yamaha '020 has as further objective to allow easier

planarization of an interlayer insulation film that has been formed on the pattern of wiring. The methods and objectives of Yamaha '020 are therefore at complete variance with the methods and objectives of the present invention asasas Yamaha '020 does not form overlying interconnect systems with the implied capability of extensive wire re-routing but forms a relatively complex sequence of material depositions (silicon oxide over which silicon nitride over which silicon oxide over which titanium over which titanium nitride over which tungsten) the sequence and composition of which is aimed at achieving the above stated Yamaha '020 objectives. The levels of metallization systems of the present invention are not part of Yamaha '020, Yamaha '020 further does not mention the use of a thick layer of passivation that overlays a relatively thick layer of passivation whereby these latter two layers are used to form overlying interconnect systems.

Similar comments as previously have been made with respect to Yamaha '020 also apply to Wolf and Cronin whereby furthermore the use of a particular material, such as polyimide for a inter metal dielectric for an application that is at complete variance with the application of the present invention, does not negate the valid application of such a material by the present

invention without invalidating the value or uniqueness of the present application.

SUMMARY

While related patents disclose processes and materials that are similar to the processes and the procedures of the invention, the combination of the processes and materials of the invention are considered unique in forming a semiconductor structure that can be created in a cost effective manner and that has not previously been claimed by related patents. There is neither disclosed nor claimed within portions of prior art of record that has been employed in rejecting applicant's claims to applicant's invention of creating top metal levels for high performance semiconductor structures in accordance with applicant's methods and materials claimed.

CONCLUSION

Based on the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 914-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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